ABSTRACT OF THE DISCLOSURE

A clock synchronization circuit includes a first delay circuit for delaying a clock signal and outputting the delayed clock signal, first and second bidirectional delay circuit strings, a first pre-stage delay circuit and a first post-stage delay circuit of variable delay time type, arranged in a pre-stage and a post-stage of the first bidirectional delay circuit string (BDDA), a second pre-stage delay circuit and a second post-stage delay circuit of variable delay time type, arranged in a pre-stage and a post-stage of the second bidirectional delay circuit string (BDDB), and a multiplexer, supplied with and multiplexing outputs of the first and second post-stage delay circuits to output the resulting signals. An output signal of the first delay circuit is supplied in common to the first and second pre-stage delay circuits. A first path composed of the first pre-stage delay circuit, first bidirectional delay circuit string and the first post-stage delay circuit and a second path composed of the second pre-stage delay circuit, second bidirectional delay circuit string and the second post-stage delay circuit are alternately switched in an interval of one cycle of the clock signal.